Characterization of AlSb/InAs surfaces and resonant tunneling devices

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We have studied the evolution of AlSb-on-InAs(001) surfaces and interfaces grown by molecular-beam epitaxy using *in situ* scanning tunneling microscopy. We find that forming InSb-like interfacial bonds on an InAs(001)-(2×4) surface creates surface roughness because the surface In coverage inherent to the (2×4) reconstruction is insufficient to form a complete InSb(001)-(1×3)-like surface layer. This morphological roughness can be eliminated by depositing additional In to compensate for the different compositions of the reconstructions. We have also grown three different 5-monolayer-thick films of AlSb on the InSb-like interface to study the effect of growth conditions on the film surface morphology. The AlSb surface can be improved by either raising the growth temperature or by growing the film using migration-enhanced epitaxy. Finally, we present electrical characterization of InAs/AlSb/GaSb resonant interband tunneling devices fabricated with different growth procedures. The possible effects of various growth procedures on interfacial quality and device properties are discussed. [S0734-211X(99)05404-9]

I. INTRODUCTION

The formation of high-quality interfaces between the nearly lattice matched ''6.1 Å'' family of III–V semiconductors, InAs, GaSb, and AlSb, is an important step in the development and fabrication of electronic and electro-optic devices from this material system. These materials have been used to make both type-I resonant tunneling diodes (RTDs) and type-II resonant interband tunneling diodes (RITDs) that show great promise for high-speed (terahertz) electronics.[1,2] Whereas the RTDs use InAs for both the cladding and quantum well material and AlSb for the tunneling barriers, the RITDs use GaSb instead as the quantum well material. In both cases the AlSb barrier layers are typically very thin, $\leqslant 5$ monolayer (ML), and the transmission coefficient for electrons to tunnel through both barriers is strongly peaked for particular energies. Accordingly, the electrical properties of these structures may be sensitive to both submonolayer fluctuations in the barrier thickness and atomic-scale compositional variations across the interfaces.[1,3,4] The incorporation of these structures into reliable high-speed circuits therefore requires an understanding of how to create smooth and abrupt interfaces with minimal interfacial disorder.

Interfacial disorder is caused by both kinetics and thermodynamics, and can be characterized by two components. When discussing interfacial disorder, we generally distinguish between morphological *roughness*, i.e., nanoscale variations in the position of the interface, and *intermixing*, i.e., fluctuations in the chemical composition on the atomic scale. Roughness is typically associated with surface topography that has evolved during the growth. When epitaxial growth does not occur in a step-flow manner, but proceeds instead by the nucleation and growth of islands on the surface, islands present at the time an interface is formed will cause interfacial roughness. The second component, intermixing, may occur *during* growth due to local disorder or inter-atomic exchange, or *after* an interface is formed due to thermodynamically driven interdiffusion. Although in some cases compositional variations may be favorable, by helping to reduce strain at the interface, for example, more often the ill-defined interfaces resulting from such disorder are expected to degrade device performance.

In previous work, we employed *in situ* scanning tunneling microscopy (STM) to characterize the surfaces that evolve during the growth of AlSb/InAs RTD-like structures by molecular-beam epitaxy (MBE).[5] We found that exposing an InAs surface to a Sb_2 flux creates a bilevel surface with vacancy islands covering ~25% of the surface. Upon further deposition of AlSb and then InAs layers on top of such a bilevel surface, the surface roughness due to islanding increased with each successive layer. Here, we describe our efforts to improve these growth surfaces and interfaces by understanding the atomic-scale structures that arise during growth, and thereby develop growth procedures that minimize interfacial roughness (although not necessarily intermixing, which we are also presently in the process of characterizing). Furthermore, we have begun to examine how these new procedures affect the electrical characteristics of functional RITDs.

II. EXPERIMENT

The experiments were carried out in an interconnected, multichamber ultrahigh vacuum facility that includes a solid-

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source MBE chamber equipped with reflection high-energy electron diffraction (RHEED), and a surface analysis chamber equipped with a STM.[6] All samples for STM study were grown without intentional doping on InAs(001) substrates using ''cracked'' arsenic and antimony. Growth rates for InAs and AlSb were calibrated by RHEED intensity oscillations. Following oxide removal, ~0.5-μm-thick InAs buffer layers were grown with a 5:1 beam equivalent pressure ratio of As:In at 1 ML/s, with 30 s interrupts under As_2 every 90 s. The substrate temperature during the buffer layer growth was approximately equal to the congruent sublimation temperature of InAs, estimated to be 470 °C. We have previously shown that by gradually reducing the As_2 flux during a 10 min interrupt following growth of the buffer layer, an island-free InAs surface is produced with a well-ordered As-terminated (2×4) reconstruction.[5]

After completion of the InAs buffer layer, the substrate temperature was reduced and AlSb growth was initiated by forming InSb interfacial bonds via migration-enhanced epitaxy (MEE). A layer of In was first deposited on the clean, As-terminated InAs surface, followed by a brief Sb_2 exposure. For example, the following shutter sequence would be used at the end of the 10 min interrupt: close the As shutter, open the In shutter for 1 s (1 ML), then open the Sb_2 shutter for 2 s. Next, a 5-ML-thick AlSb film was deposited on the InSb-like interface. Three different growth procedures for this layer were examined, including different growth temperatures, as will be described later. In each case, after depositing the 5 ML AlSb film a 15 s interrupt under Sb_2 was performed, and then the sample was allowed to cool to room temperature. In a RTD or RITD structure, these AlSb surfaces would represent possible starting surfaces upon which the InAs or GaSb quantum well material would be deposited. Immediately following the completion of each growth, the samples were removed from the MBE chamber and transferred *in vacuo* to the surface analysis chamber (base pressure $<1\times10^{-10}$ Torr), as described previously.[5] All STM images shown here were acquired in constant-current mode with sample biases ranging from −1.2 to −3.3 V and tunneling currents between 30 pA and 0.7 nA.

As a first step to correlating device performance with growth procedures specifically developed using the results of our surface and interface characterization, we have fabricated several complete InAs/AlSb/GaSb RITD structures on both InAs and GaAs substrates. For each substrate type, two samples were grown: one using a ''conventional'' growth procedure, and the other implementing a number of changes in the growth intended to affect interfacial structure. All four RITD samples were grown at ~440 °C, and consist of a 9 nm (30 ML) GaSb quantum well between two 1.5 nm (5 ML) AlSb barriers. Silicon was used as a *n*-type dopant for all the doped layers of the structure. For the InAs substrates, a 1-μm-thick InAs buffer layer doped at 3×10^{18} cm^{-3} was grown first, followed by 30 nm of InAs doped at 1×10^{17} cm^{-3}, and then 12 nm of undoped InAs. The first AlSb barrier was grown on this undoped layer, with InSb-like interfacial bonds formed using MEE. For the conventional growth, 1 ML of In+2 s Sb_2 was used during the MEE. For the alternate growth, additional In was deposited (as will be explained later). At the interface between the second AlSb barrier and the adjoining InAs layer, InSb-like bonds were also formed using MEE (with 1 ML of In). The InAs immediately on top of the second AlSb barrier was undoped for the first 12 nm, doped at 1×10^{17} cm^{-3} for the next 30 nm, and then doped at 3×10^{18} cm^{-3} for the final 0.2 μm. During the alternate growth procedure, in addition to using additional In during formation of the first AlSb/InAs interface, 100 s interrupts were added after the growth of the first AlSb barrier layer, the GaSb quantum well, and the second AlSb barrier. Similar RITD samples were grown on the semi-insulating GaAs substrates; the only difference is that a 0.2-μm-thick AlSb buffer layer and 0.5 μm of undoped InAs were grown before the doped InAs buffer layer. After growth, standard photolithography procedures were used to fabricate an array of gold ohmic contacts that also served as an etch mask for the formation of mesa RITDs. Current density-versus-voltage spectra were then recorded at room temperature for devices from each sample.

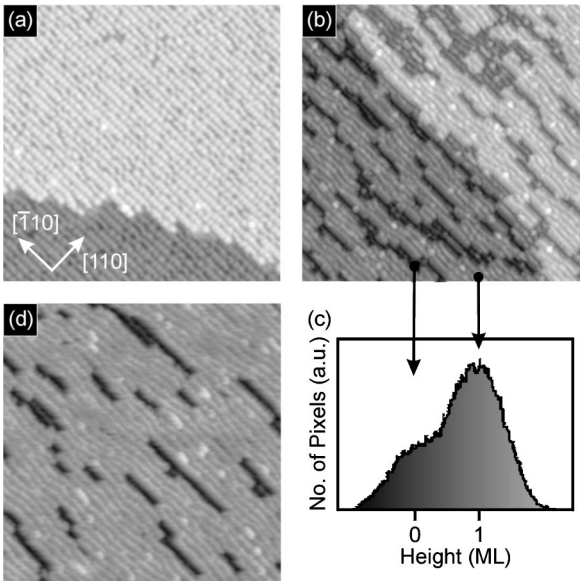

FIG. 1. Filled-state STM images (60 nm×60 nm) of (a) clean InAs(001)-(2×4); (b) InAs after depositing 1 ML of In and exposing to 2 s of Sb_2; and (d) InAs after depositing about 1.25 ML of In and exposing to 2 s of Sb_2. The height histogram for a single substrate terrace on the surface shown in (b) is displayed in (c).

III. RESULTS AND DISCUSSION

A typical STM image of the InAs buffer layer surface (after the 10 min interrupt) is shown in Fig. 1(a). The surface is nearly ideal, composed of atomically smooth terraces separated by monolayer-height (3 Å) steps. As previously reported, micron-scale images show that the terraces are ~0.5 μm wide with essentially no islands.[5] On the atomic scale, the surface exhibits a well-ordered (2×4) reconstruction, consistent with the sharp diffraction spots observed in the RHEED. Atomic resolution images (not shown) are simi-

lar in appearance to those previously reported for the As-terminated InAs and GaAs(001)-(2×4) surfaces, and are consistent with the generally accepted $\beta 2(2\times4)$ model for this reconstruction.[7] In this model, the surface III–V layer is nonstoichiometric, consisting of 1/2 ML of As on top of 3/4 ML of In. The 1/2 ML of As is in the form of dimers with each dimer bond oriented in the [110] direction. Pairs of these dimers align in rows along the [110] direction [the rows visible in Fig. 1(a)], separated by a row of single As dimers one InAs layer below.

The first interface of interest in a RITD structure is the AlSb-on-InAs interface, i.e., the interface directly before the first barrier layer. A key issue in the heteroepitaxial growth of antimonides on arsenides (or vice versa) is the type of interfacial bonds that are formed. For AlSb/InAs, the interfacial bonds can be either InSb-like or AlAs-like. For a number of reasons, including the general observation that InSb-like interfacial bonds lead to more abrupt interfaces,[8–11] we usually prepare our interfaces with this bond type. When this interfacial layer is created from the InAs starting surface by MEE (1 ML of In followed by 2 s of Sb_2), the RHEED pattern changes from the sharp (2×4) of clean InAs, to a streaky (1×3). Although we expect that the surface formed in this way should be terminated primarily with Sb, there may still be some remnant As present. [We will refer to this surface henceforth as the InSb(As) surface or interface.] An image of such a surface is displayed in Fig. 1(b). As discussed previously,[5] these surfaces exhibit a disordered (1×3)-like reconstruction with vacancy islands covering a quarter of the surface. The bifurcation of the surface into two levels is shown quantitatively in Fig. 1(c) by the height histogram for a single substrate terrace.

The (1×3)-like reconstruction of this InSb(As) surface is similar in appearance to that observed for other III–Sb materials. Based on our work[5] and previously reported results and models,[12–14] we believe the InSb(As) surface has a structure like the $(1\times3)/c(2\times6)$ reconstruction proposed for the clean III–Sb surfaces: a full plane (1 ML) of group III atoms covered by 1 2/3 ML of group V atoms (in this case possibly Sb and As). We have demonstrated elsewhere that the formation of vacancy islands is a direct result of the different compositions of the clean InAs (0.5 ML As/0.75 ML In) and Sb-terminated surfaces (~1.7 ML Sb+As/1 ML In).[15] When depositing 1 ML of In during MEE, one can think of 1/4 ML of this In ''filling in'' the In missing from the original (2×4)-reconstructed surface, while the other 3/4 ML remains as additional islands on the surface. Terminating this In with Sb, to complete the Sb-rich (1×3)-like reconstruction, leads to the observed 75%/25% bilevel surface morphology. Given this understanding of the vacancy island formation, and *additional* 0.25 ML of In can be added during the MEE procedure to compensate for the different compositions of the reconstructions. The much smoother morphology that results is shown in Fig. 1(d). For this growth the vacancy island coverage has been reduced to <7%. The primary limitation to getting a flat surface is depositing the precise amount of In which is needed.[15]

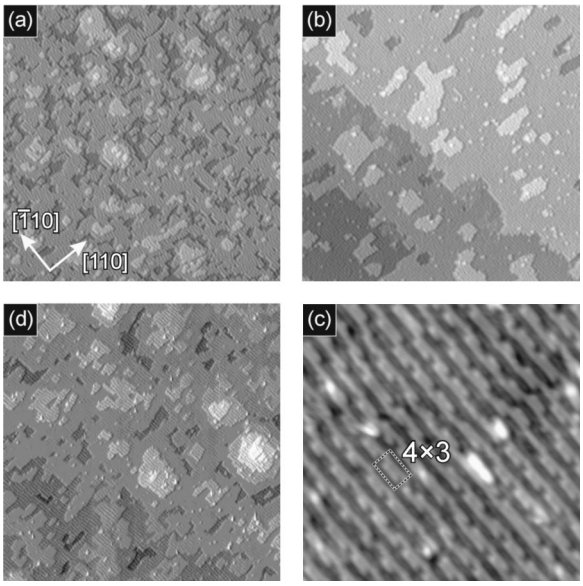

FIG. 2. Filled-state images of a 5-ML-thick AlSb film grown on a surface like that shown in Fig. 1(d). (a) Grown at 400 °C. (b) Grown at 470 °C. A higher resolution image of this surface, 17 nm×17 nm, is shown in (c). (d) Grown with layer-by-layer MEE at 400 °C. Images (a), (b), and (d) are 130 nm×130 nm, and have a gradient component added to the gray scale to accent the step edges.

We now proceed to examine the second interface—the one between the first AlSb barrier and the InAs or GaSb quantum well material. Three 5-ML-thick AlSb films were grown under different conditions, each starting on a flat, freshly prepared InSb(As) surface made using 1.25 ML of In, as just described. The first film was grown at 400 °C using a constant growth rate of 0.5 ML/s, producing the morphology shown in Fig. 2(a). The surface has a disordered (1×3)-like reconstruction and primarily consists of three different levels per substrate terrace, covering 21%, 67%, and 11% of each terrace (lowest to highest). It is apparent that the growth of the AlSb film is proceeding via island growth, not step flow, consistent with the observation of RHEED intensity oscillations during the growth. This growth mode is not surprising given that 400 °C is a relatively low temperature for AlSb growth.

To explore the effect of growth temperature on the AlSb film morphology, the second AlSb film was grown at the same growth rate as the previous sample, but at the InAs growth temperature of ~470 °C. As shown in Fig. 2(b), there is a dramatic change in the film surface morphology. The surface is still composed of three levels per terrace but is much smoother, with islands and vacancies comprising 17% and 3% of the surface, respectively. The growth is getting close to step flow due to the increased diffusion lengths at this higher temperature. The surface is also better ordered on the atomic scale, having relatively kink-free dimer rows [Fig. 2(c); compare with Fig. 4(c) in Ref. 5]. Based solely on its topography, this surface would appear to be a better starting point for the adjacent quantum well. However, it is important to recall that a variety of both kinetically and thermodynamically driven processes occur during epitaxy. For example,

the higher growth temperature may increase the amount of interfacial intermixing, or promote the formation of extended dislocations in a strained heterostructure. Thus, whereas the growth of AlSb at this higher temperature produces a much smoother growth surface, it ultimately may or may not lead to better device performance.

An interesting consequence of the increased atomic scale order on the AlSb film surface grown at higher temperature is the observation of a periodic ''defect'' that occurs in the surface Sb dimer rows within the supposed $c(2\times6)$ reconstruction. As shown in Fig. 2(c), in filled-state images it appears as if one Sb atom (half a dimer) is missing from every fourth dimer along the [110] direction, giving the most well-ordered regions of the surface an overall (4×3) symmetry. Interestingly, hints of this structure are also apparent upon close inspection of previously published atomic-scale images of AlSb(001),[5,14] suggesting that this (4×3) structure may, in fact, be a low-energy reconstruction. Further investigations, both experimental and theoretical, are in progress with the goal of definitively determining the (4×3) structure and stability.

Because it may be advantageous to grow arsenide-antimonide heterostructures at relatively low temperatures (<450 °C), we have investigated whether the otherwise kinetically limited AlSb film morphology can be improved using layer-by-layer MEE growth. Specifically, the third of our 5-ML-thick AlSb films was grown by alternately depositing 1 ML of Al (2 s at 0.5 ML/s) and 5 s of Sb_2 repeated five times. Depositing the Al in the absence of a Sb_2 flux is expected to increase the diffusion length of Al adatoms, and the short interrupts under Sb_2 should help to coarsen any islands and thereby smooth the surface further. These effects are indeed apparent in the resulting surface morphology, shown in Fig. 2(d). Compared to the surface grown without the interrupts at the same temperature, Fig. 2(a), this surface has generally larger islands and fewer vacancies (i.e., the lower level on each terrace, whose area is reduced from 21% to 10%). Although the effectively lower growth rate and periodic interrupts improve the surface morphology, it should be noted that there might also be some problems created by this growth procedure. One problem is that the thickness of the layer could be more susceptible to flux transients or ''bursts'' that arise when a shutter is opened. Another issue is the longer growth times, during which the detrimental incorporation of dopant-like impurities into the active layers could become significant.

As a first step in exploring how growth procedures affect device characteristics, we have characterized full RITD structures fabricated using a number of procedures developed to reduce interfacial roughness. As described in Sec. II, one sample was grown on each substrate (GaAs and InAs) using conventional methods, i.e., the AlSb-on-InAs interface was formed by MEE using 1 ML of In. We will denote these samples ''GaAs–A'' and ''InAs–A.'' A second pair of samples, ''GaAs–B'' and ''InAs–B,'' was prepared using 1.25 ML of In (to produce a flatter AlSb-on-InAs interfacial layer), plus additional 100 s interrupts after the growth of each barrier layer and quantum well. Typical current–voltage spectra for InAs–A and InAs–B RITDs are displayed in Fig. 3. The spectra exhibit characteristic resonant tunneling behavior, with peak currents near ±130 mV and valley currents in the vicinity of ±350–400 mV. (The sharp features between the peaks and valleys are due to bistability effects.) Note that at positive bias the top of the mesa is positive with respect to the substrate side of the device. In general, we observed little difference in the negative current densities between sample sets for either substrate; however, the positive current densities are consistently lower for the samples with modified interfaces (the ''B'' samples). For example, the positive bias peak current density is $\sim2.5\times10^4$ A/cm^2 for InAs–A RITDs, and $\sim2.2\times10^4$ A/cm^2 for the InAs–B in Fig. 3 (values very similar to those previously reported for similar RITD structures).[16,17] Because both peak and valley currents decreased about the same amount, the peak-to-valley ratio, often used as a figure of merit for RITDs, did not change significantly. Considering the differences in the peak currents between the A and B samples relative to the variations in peak currents across both samples, the different interface treatments did not significantly affect the peak current densities or peak-to-valley ratios.

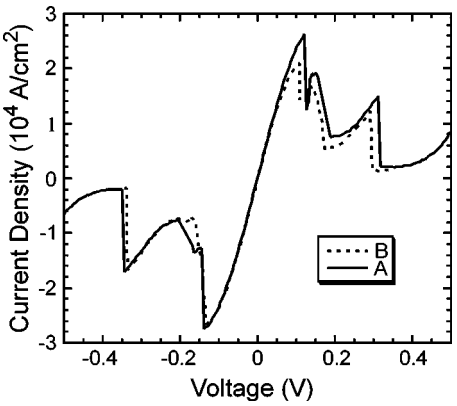

FIG. 3. Current density as a function of bias voltage acquired at room temperature for 3 μm diameter mesa RITDs grown on InAs substrates. The peak and valley currents are at approximately ±130 and ±300 mV, respectively, with positive bias corresponding to the mesa at a positive voltage with respect to the substrate. The sharp features between the peak and valley are due to bistability effects. Sample A was grown using conventional procedures, and sample B with a number of changes expected to reduce interfacial roughness.

The ratio of the peak current for positive bias to the peak current for negative bias, I_+/I_-, is an alternate characteristic of RITDs that provides a rough measure of the asymmetry in the structure along the growth direction. When the growth does not produce a structure with a mirror plane in the center of the GaSb well, $I_+/I_-\neq1$. Because different methods were used to prepare all the interfaces within the A and B samples, it is reasonable to expect that I_+/I_- will vary. The average values and standard deviations of I_+/I_- measured for devices at many locations on the samples, with mesa diameters ranging from 2 to 20 μm, are the following: InAs–A=0.95±0.06, InAs–B=0.78±0.03, GaAs–A=0.84

± 0.01, and GaAs–B$=0.65\pm 0.01$. On both substrates the ratio is consistently smaller for the samples with specially treated interfaces. This effect is mainly associated with a reduction in the size of the peak current at positive bias (see Fig. 3). However, because the growth procedures for all four interfaces within the RITD structure were changed from A to B, the decrease in peak current density is a convolution of the effects of the changes to all the interfaces. At this time, we do not know how all these growth modifications lead to the asymmetries in current–voltage measurements that we have observed. One possibility is that the extra In used at the first interface may be changing the effective band offset at the first barrier, thereby reducing the forward tunneling current. Alternately, the additional growth interrupts may somehow change the dominant scattering mechanisms at the interfaces or the overall tunneling probabilities. The greater problem that remains is to develop methods that will result in enhanced peak current densities.

IV. CONCLUSIONS

We have used *in situ* STM to study the surfaces and interfaces that evolve during the MBE growth of AlSb on InAs(001). We have discovered that the change in surface reconstruction that occurs across the III–Sb/III–As interface creates interfacial roughness. Specifically, when forming InSb-like interfacial bonds on an InAs(001)-(2×4) surface, vacancy islands emerge because the surface In coverage is insufficient to form a complete InSb(001)-(1×3)-like surface layer. This roughness can be greatly reduced by depositing the appropriate amount of additional In to compensate for the compositional differences between the reconstructions. We have also deposited 5-ML-thick AlSb films on the flatter InSb-like interfacial surface using three different growth conditions. The AlSb film surface morphology significantly improves when the AlSb is grown at higher temperature, as expected. We find it is also possible to reduce the island density at lower substrate temperatures by growing the AlSb film layer-by-layer using MEE. Atomic resolution images of the well-ordered AlSb surfaces resulting from higher temperature growth reveal periodic defects in the surface Sb dimer rows along the [110] directions that give the surface reconstruction an overall (4×3) symmetry.

We have begun to implement some of the growth techniques aimed at reducing interfacial roughness into RITDs. Current–voltage spectra were acquired for RITDs that were fabricated using either 1 or 1.25 ML of In during the MEE at the AlSb-on-InAs interface. In addition, 100 s growth interrupts were added at the other interfaces. In general, the devices with specially treated interfaces had slightly different electrical characteristics (slightly lower current densities at positive bias). Although we have not yet correlated changes in device performance with particular changes in interfacial structure, it is clear that such an understanding can be achieved by closely coordinating surface and interface characterization with device fabrication and testing.

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